ABSTRACT OF THE DISCLOSURE

A driver circuit of a display device, which includes TFTs of a single conductivity type and outputs an output signal with normal amplitude. A pulse is inputted to TFTs 101 and 104 to turn ON the TFTs and a potential of a node α is raised. When the potential of the node α reaches (VDD – VthN), the node α becomes in a floating state. Accordingly, a TFT 105 is turned ON and a potential of an output node is raised as a clock signal becomes High level. On the other hand, a potential of a gate electrode of the TFT 105 is further raised due to an operation of a capacitance means 107 as the potential of the output node is raised, so that the potential of the gate electrode of the TFT 105 becomes higher than (VDD + VthN). Thus, the potential of the output node is raised to VDD without causing a voltage drop due to a threshold voltage of the TFT 105. An output at the subsequent stage is then inputted to a TFT 103 to turn the TFT 103 ON, while the potential of the node α of TFTs 102 and 106 is dropped to turn the TFT 105 OFF. As a result, the potential of the output node becomes Low level.